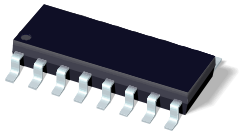
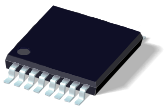




2x2 LVPECL CROSSPOINT SWITCH

FEATURES

- **High Speed 2x2 LVPECL Crosspoint Switch**
- **LVDS Crosspoint Switch Available in SN65LVCP22**
- **50 ps (Typ), of Peak-to-Peak Jitter With PRBS = 2^{23}– 1 Pattern**
- **Output (Channel-to-Channel) Skew Is 10 ps (Typ), 50 ps (Max)**
- **Configurable as 2:1 Mux, 1:2 Demux, Repeater or 1:2 Signal Splitter**
- **Inputs Accept LVDS, LVPECL, and CML Signals**
- **Fast Switch Time of 1.7 ns (Typ)**
- **Fast Propagation Delay of 0.75 ns (Typ)**
- **16 Lead SOIC and TSSOP Packages**
- **Operating Temperature: –40°C to 85°C**

APPLICATIONS

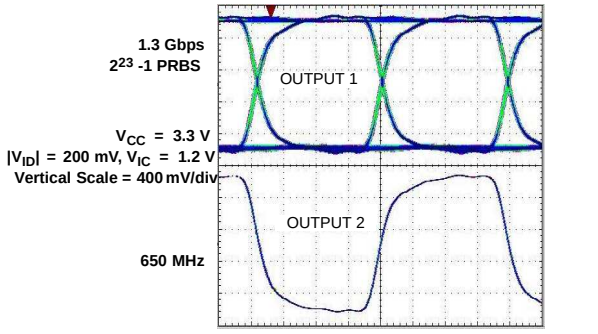
- **Gigabit Ethernet Redundant Transmission Paths**
- **Gigabit Interface Converters (GBICs)**
- **Fibre Channel Redundant Transmission Paths**
- **HDTV Video Routing**
- **Base Stations**
- **Protection Switching for Serial Backplanes**
- **Network Switches/Routers**
- **Optical Networking Line Cards/Switches**
- **Clock Distribution**

DESCRIPTION

The SN65LVCP23 is a 2x2 LVPECL crosspoint switch. The dual channels incorporate wide common-mode (0 V to 4 V) receivers, allowing for the receipt of LVDS, LVPECL, and CML signals. The dual outputs are LVPECL drivers to provide high-speed operation. The SN65LVCP23 provides a single device supporting 2:2 buffering (repeating), 1:2 splitting, 2:1 multiplexing, 2x2 switching, and LVDS/CML to LVPECL level translation on each channel. The flexible operation of the SN65LVCP23 provides a single device to support the redundant serial bus transmission needs (working and protection switching cards) of fault-tolerant switch systems found in optical networking, wireless infrastructure, and data communications systems. TI offers an additional gigabit repeater/translator in the SN65LVDS101.

The SN65LVCP23 uses a fully differential data path to ensure low-noise generation, fast switching times, low pulse width distortion, and low jitter. Output channel-to-channel skew is less than 10 ps (typ) and 50 ps (max) to ensure accurate alignment of outputs in all applications. Both SOIC and TSSOP package options are available.

OUTPUTS OPERATING SIMULTANEOUSLY



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PACKAGE DESIGNATOR	PART NUMBER(1)	SYMBOLIZATION
SOIC	SN65LVCP23D	LVCP23
TSSOP	SN65LVCP23PW	LVCP23

(1) Add the suffix R for taped and reeled carrier

PACKAGE DISSIPATION RATINGS

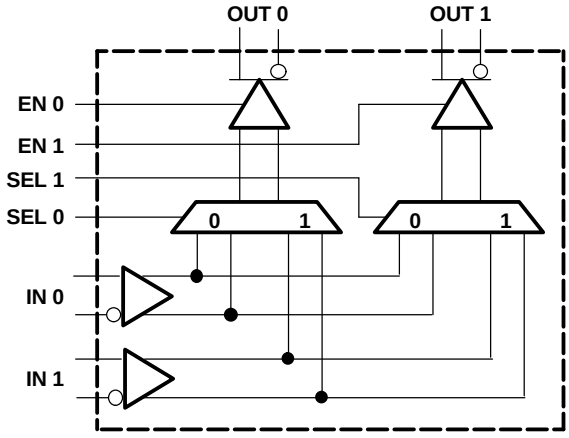
PACKAGE	CIRCUIT BOARD MODEL	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
SOIC (D)	High-K(2)	1361 mW	13.9 mW/°C	544 mW
TSSOP (PW)	High-K(2)	1074 mW	10.7 mW/°C	430 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

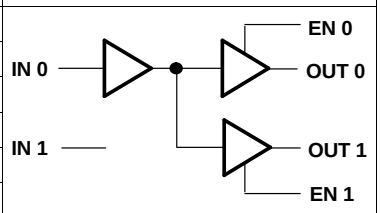
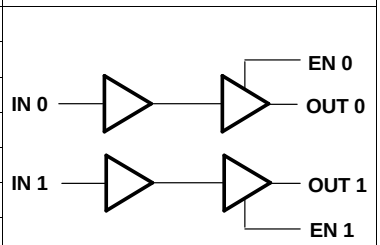
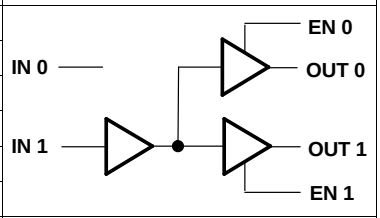
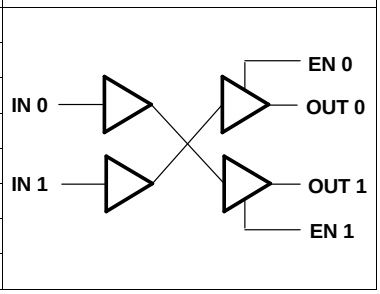
THERMAL CHARACTERISTICS

PARAMETER			TEST CONDITIONS	VALUE	UNITS
θ_{JB}	Junction-to-board thermal resistance	D		15.7	°C/W
		PW		22.1	°C/W
θ_{JC}	Junction-to-case thermal resistance	D		26.1	°C/W
		PW		17.3	°C/W
P_D	Device power dissipation	Typical	V_{CC} = 3.3 V, T_A = 25°C, 2 Gbps	165	mW
		Maximum	V_{CC} = 3.6 V, T_A = 85°C, 2 Gbps	234	mW

FUNCTIONAL BLOCK DIAGRAM

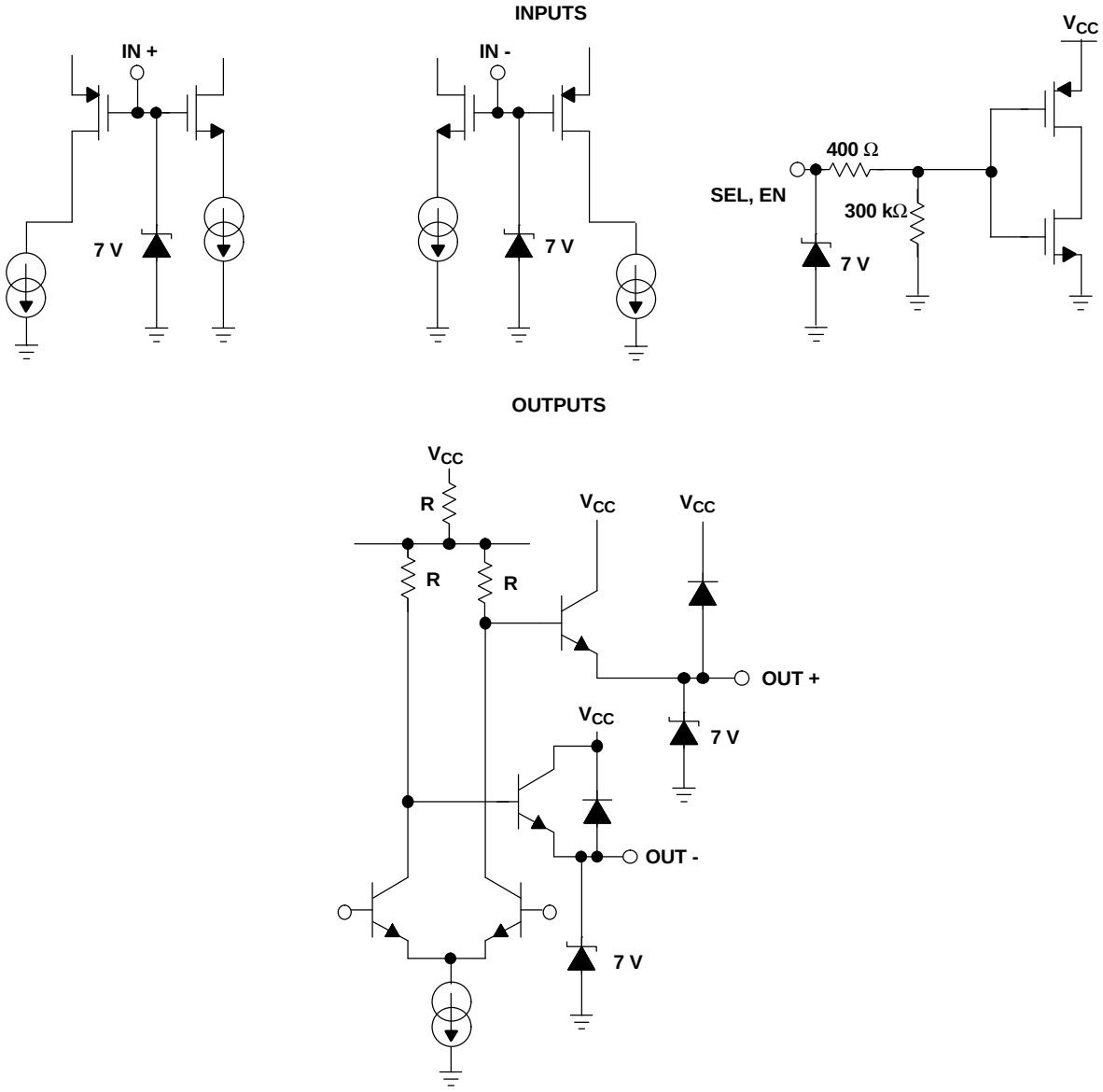


CIRCUIT FUNCTION TABLE

INPUTS(1)						OUTPUTS(1)		LOGIC DIAGRAM
IN 0	IN 1	SEL 0	SEL1	EN 0	EN 1	OUT 0	OUT 1	
X	X	X	X	L	L	L	L	
>100 mV	X	L	L	H	L	H	L	
<-100 mV	X	L	L	H	L	L	L	
<-100 mV	X	L	L	H	H	L	L	
>100 mV	X	L	L	H	H	H	H	
>100 mV	X	L	L	L	H	L	H	
<-100 mV	X	L	L	L	H	L	L	
>100 mV	X	L	H	H	L	H	L	
<-100 mV	X	L	H	H	L	L	L	
<-100 mV	<-100 mV	L	H	H	H	L	L	
<-100 mV	>100 mV	L	H	H	H	L	H	
>100 mV	<-100 mV	L	H	H	H	H	L	
>100 mV	>100 mV	L	H	H	H	H	H	
X	>100 mV	L	H	L	H	L	H	
X	<-100 mV	L	H	L	H	L	L	
X	>100 mV	H	H	H	L	H	L	
X	<-100 mV	H	H	H	L	L	L	
X	<-100 mV	H	H	H	H	L	L	
X	>100 mV	H	H	H	H	H	H	
X	>100 mV	H	H	L	H	L	H	
X	<-100 mV	H	H	L	H	L	L	
X	>100 mV	H	L	H	L	H	L	
X	<-100 mV	H	L	H	L	L	L	
<-100 mV	<-100 mV	H	L	H	H	L	L	
<-100 mV	>100 mV	H	L	H	H	H	L	
>100 mV	<-100 mV	H	L	H	H	L	H	
>100 mV	>100 mV	H	L	H	H	H	H	
>100 mV	X	H	L	L	H	L	H	
<-100 mV	X	H	L	L	H	L	L	

(1) H = High level, L = Low level, Z = High impedance, X = Don't care

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNITS
Supply voltage range,(2) V_{CC}			–0.5 V to 4 V
CMOS/TTL input voltage (ENO, EN1, SEL0, SEL1)			–0.5 V to 4 V
Receiver input voltage (IN+, IN–)			–0.7 V to 4.3 V
LVPECL driver output voltage (OUT+, OUT–)			–0.5 V to 4 V
Output current	Continuous		50 mA
	Surge		100 mA
Storage temperature range			–65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			235°C
Continuous power dissipation			See Dissipation Rating Table
Electrostatic discharge	Human body model(3)	All pins	±5 kV
	Charged-device mode(4)	All pins	±500 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminals.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
	Receiver input voltage	0		4	V
	Junction temperature			125	°C
T_A	Operating free-air temperature(1)	–40		85	°C
$\|V_{ID}\|$	Magnitude of differential input voltage	0.1		3	V

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
CMOS/TTL DC SPECIFICATIONS (EN0, EN1, SEL0, SEL1)						
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.8	V
I_{IH}	High-level input current	V_{IN} = 3.6 V or 2.0 V, V_{CC} = 3.6 V		±3	±20	µA
I_{IL}	Low-level input current	V_{IN} = 0.0 V or 0.8 V, V_{CC} = 3.6 V		±1	±10	µA
V_{CL}	Input clamp voltage	I_{CL} = –18 mA		–0.8	–1.5	V
LVPECL OUTPUT SPECIFICATIONS (OUT0, OUT1)						
V_{OH}	Output high voltage	R_L = 50 Ω to V_{TT} , V_{TT} = V_{CC} – 2.0 V, See Figure 2	V_{CC} – 1.3		V_{CC} – 0.85	V
V_{OL}	Output low voltage		V_{CC} – 2.2		V_{CC} – 1.65	
$\lvert V_{OD} \rvert$	Differential output voltage		600	800	1000	mV
C_O	Differential output capacitance	V_I = 0.4 sin(4E6πt) + 0.5 V		3		pF
RECEIVER DC SPECIFICATIONS (IN0, IN1)						
V_{TH}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V_{TL}	Negative-going differential input voltage threshold	See Figure 1 and Table 1	–100			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis			25		mV
V_{CMR}	Common-mode voltage range	V_{ID} = 100 mV, V_{CC} = 3.0 V to 3.6 V	0.05		3.95	V
I_{IN}	Input current	V_{IN} = 4 V, V_{CC} = 3.6 V or 0.0 V		±1	±10	µA
		V_{IN} = 0 V, V_{CC} = 3.6 V or 0.0 V		±1	±10	
C_{IN}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		1		pF
SUPPLY CURRENT						
I_{CCD}	DC supply current	No load		50	65	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

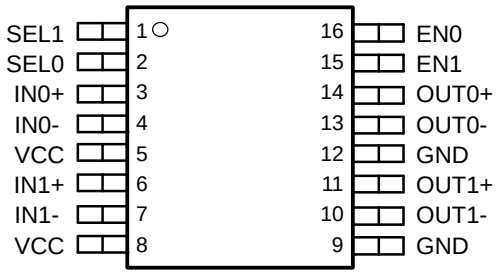
over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SET}	Input to SEL setup time	Figure 5	1	0.5		ns
t_{HOLD}	Input to SEL hold time	Figure 5	1.1	0.5		ns
t_{SWITCH}	SEL to switched output	Figure 5		1.7	2.5	ns
t_{PHKL}	Disable time, high-level-to-known LOW	Figure 4		2	2.5	ns
t_{PKLH}	Enable time, known LOW-to-high-level output	Figure 4		2	2.5	ns
t_{LHT}	Differential output signal rise time (20% – 80%)(1)	Figure 3	80	110	220	ps
t_{HLT}	Differential output signal fall time (20% – 80%)(1)	Figure 3	80	110	220	ps
t_{JIT}	Added peak-to-peak jitter	V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 650 MHz		15	30	ps
		V_{ID} = 200 mV, PRBS = 2^{23}–1 data pattern and K28.5 (0011111010), V_{CM} = 1.2 V at 1.3 Gbps		50	100	ps
t_{Jrms}	Added random jitter (rms)	V_{ID} = 200 mV, 50% duty cycle, V_{CM} = 1.2 V, 650 MHz		0.3	0.5	ps_{RMS}
t_{PLHD}	Propagation delay time, low-to-high-level output(1)	V_{CC} = 3.3 V, T_A = 25°C, See Figure 3	400	750	1100	ps
t_{PHLD}	Propagation delay time, high-to-low-level output(1)	V_{CC} = 3.3 V, T_A = 25°C, See Figure 3	400	750	1100	ps
t_{skew}	Pulse skew ($\lvert t_{PLHD} - t_{PHLD} \rvert$)(2)	Figure 3		20	100	ps
t_{CCS}	Output channel-to-channel skew, splitter mode	Figure 3		10	50	ps
f_{MAX}	Maximum operating frequency(3)		1			GHz

(1) Input: V_{IC} = 1.2 V, V_{ID} = 200 mV, 50% duty cycle, 1 MHz, t_r/t_f = 500 ps
(2) t_{skew} is the magnitude of the time difference between the t_{PLHD} and t_{PHLD} of any output of a single device.
(3) Signal generator conditions: 50% duty cycle, t_r or $t_f \le 100$ ps (10% to 90%), transmitter output criteria: duty cycle = 45% to 55% $V_{OD} \ge$ 300 mV.

PIN ASSIGNMENTS

D or PW PACKAGE
(TOP VIEW)



PARAMETER MEASUREMENT INFORMATION

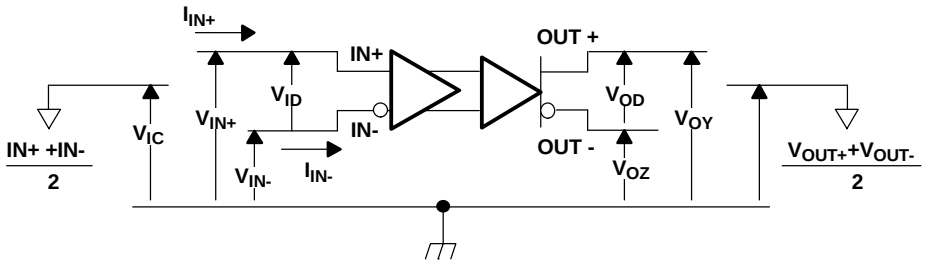


Figure 1. Voltage and Current Definitions

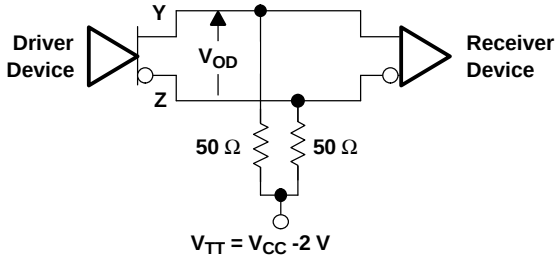
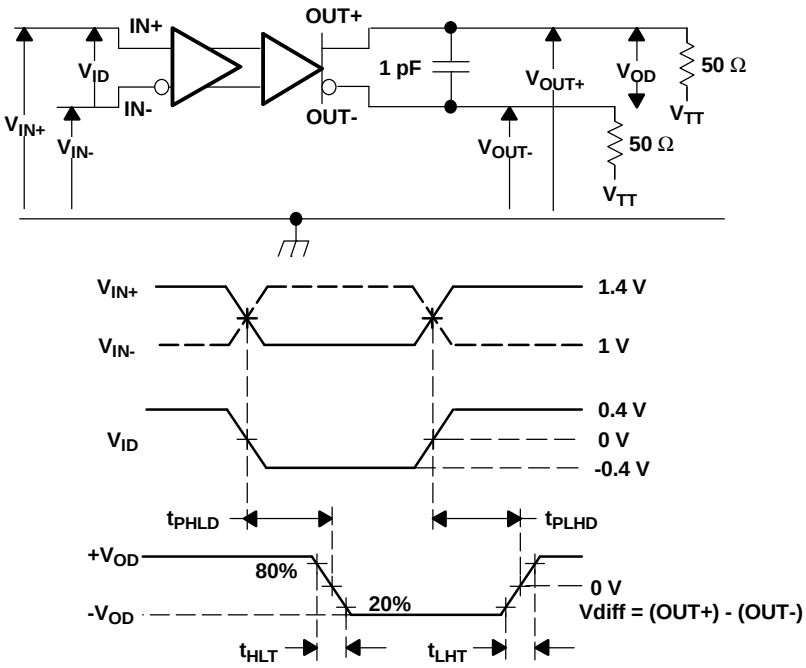


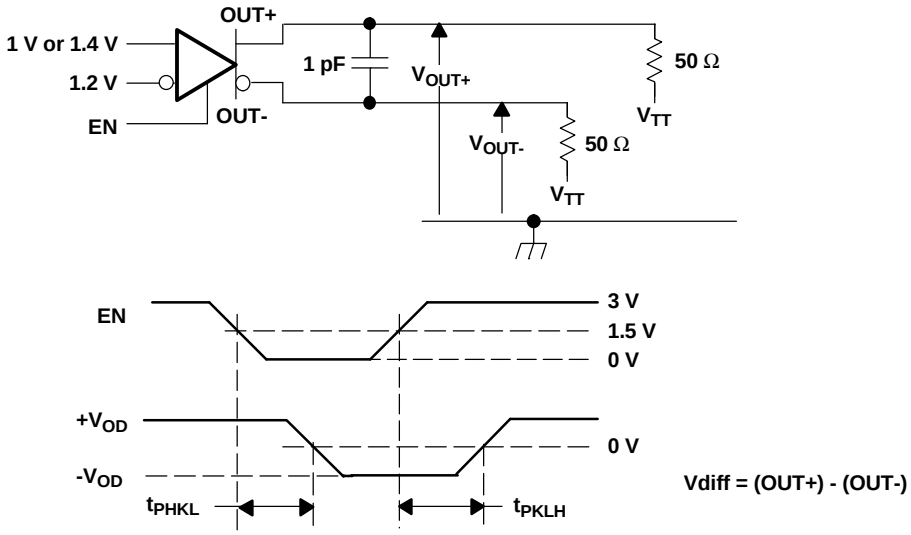
Figure 2. Typical Termination for LVPECL Output Driver



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 0.25$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 3. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



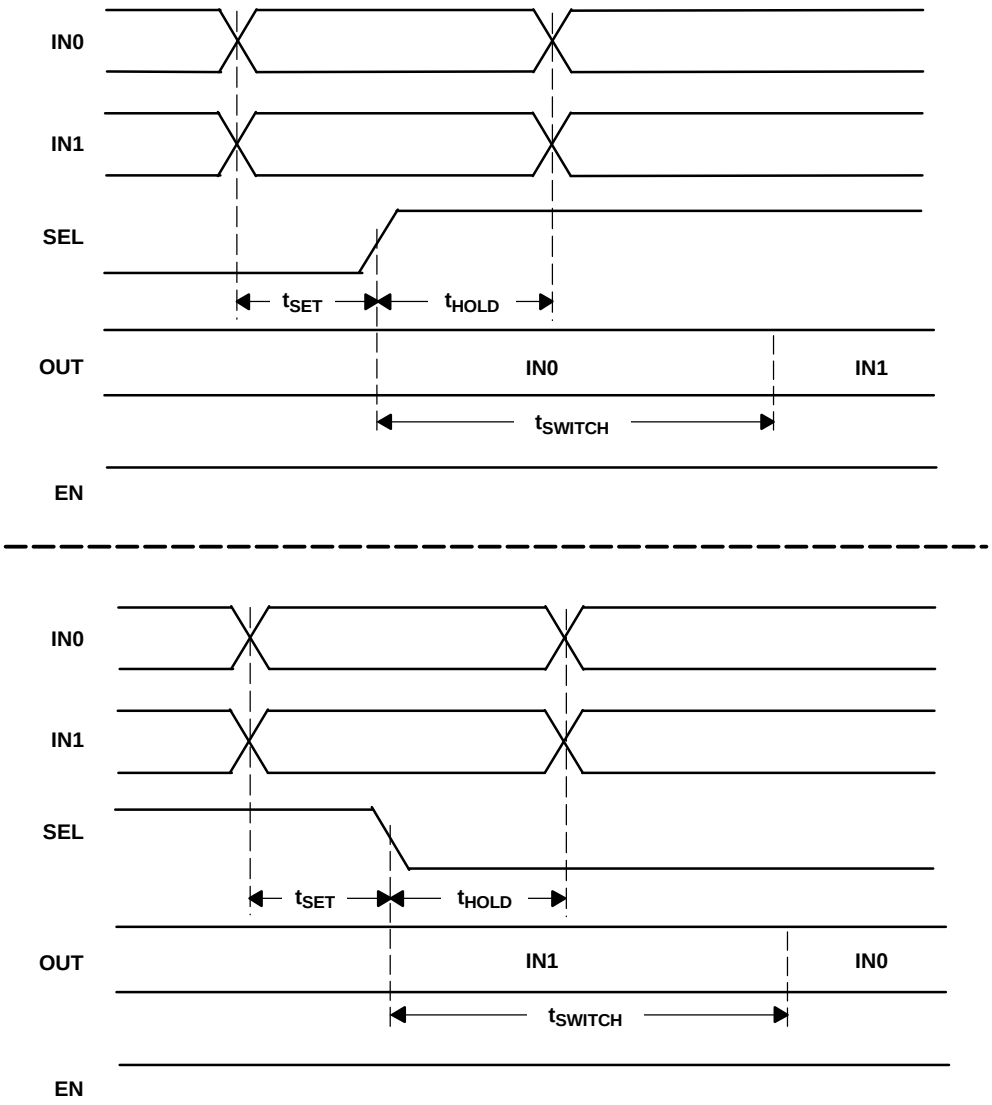
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns, C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Enable and Disable Time Circuit and Definitions

Table 1. Receiver Input Voltage Threshold Test

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	–100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4. 0 V	–100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	–100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	–1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	–1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	–1000 mV	0.5 V	L

(1) H = high level, L = low level



NOTE: t_{SET} and t_{HOLD} times specify that data must be in a stable state before and after mux control switches.

Figure 5. Input to Select for Both Rising and Falling Edge Setup and Hold Times

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

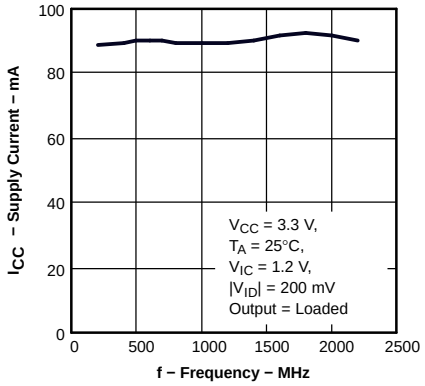


Figure 6.

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

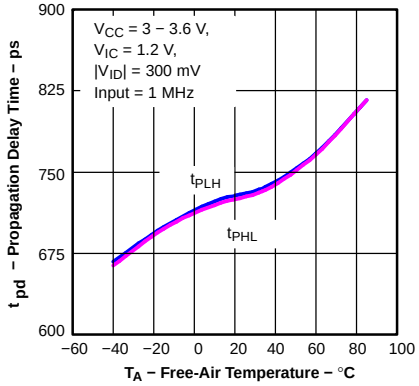


Figure 7.

PEAK-TO-PEAK JITTER vs FREQUENCY

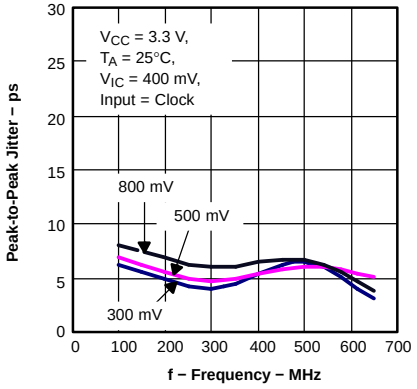


Figure 8.

PEAK-TO-PEAK JITTER vs DATA RATE

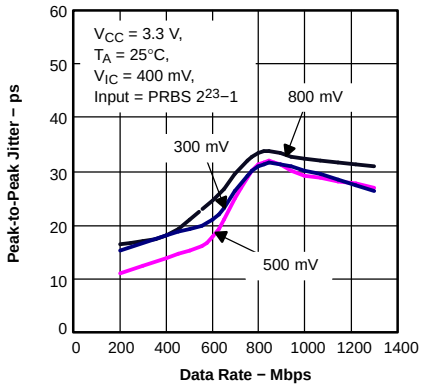


Figure 9.

PEAK-TO-PEAK JITTER vs FREQUENCY

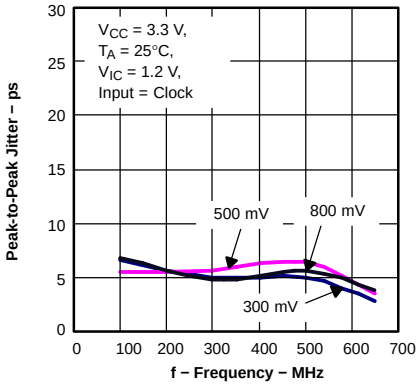


Figure 10.

PEAK-TO-PEAK JITTER vs DATA RATE

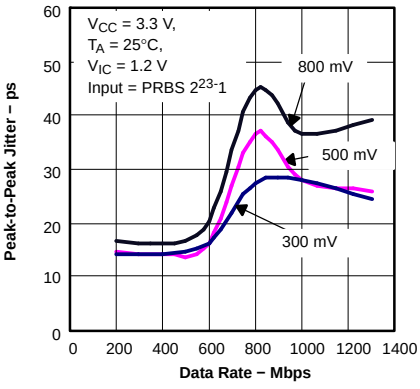


Figure 11.

PEAK-TO-PEAK JITTER vs FREQUENCY

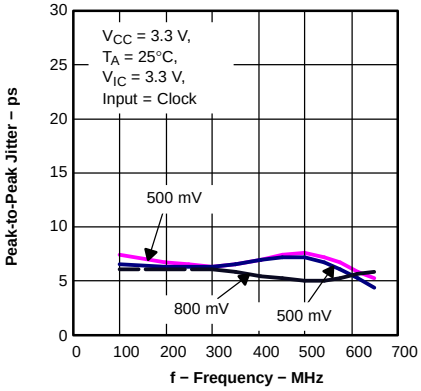


Figure 12.

PEAK-TO-PEAK JITTER vs DATA RATE

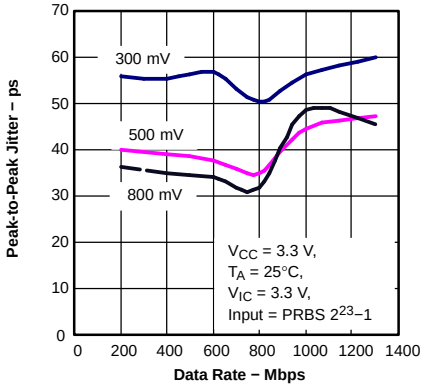


Figure 13.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL OUTPUT VOLTAGE vs FREQUENCY

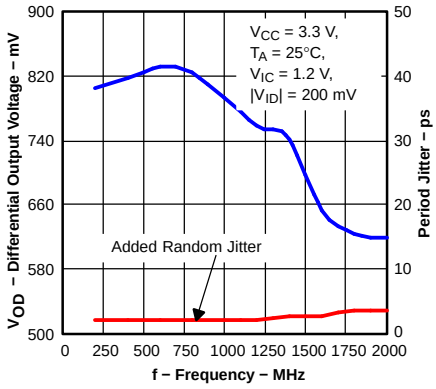


Figure 14.

PEAK-TO-PEAK JITTER vs DATA RATE

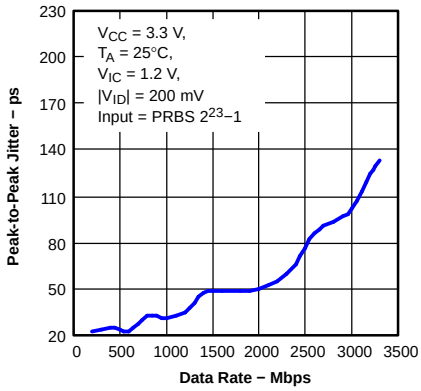


Figure 15.

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

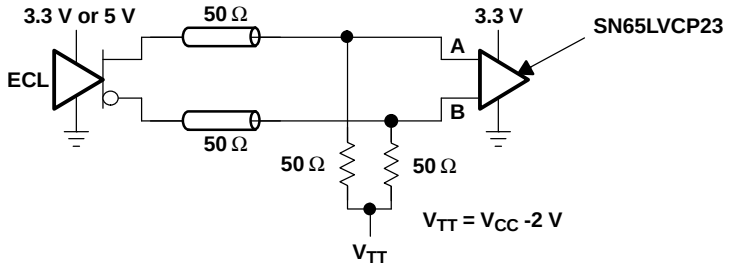


Figure 16. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

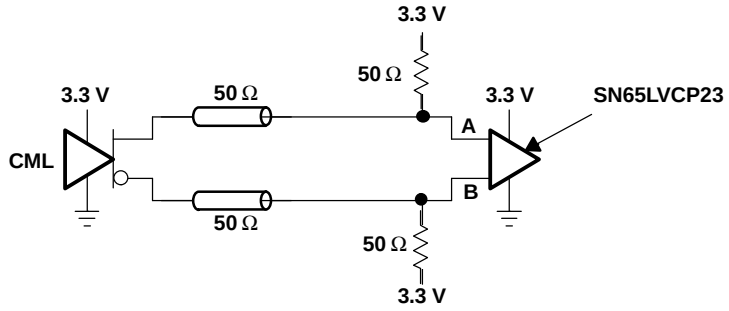


Figure 17. Current-Mode Logic (CML)

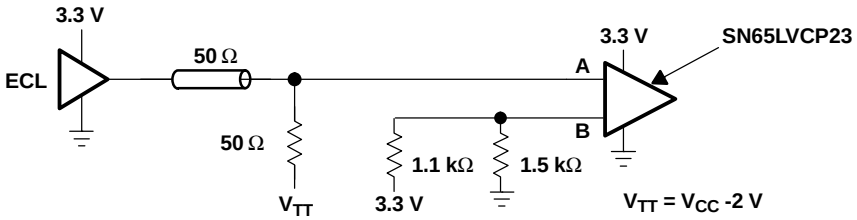


Figure 18. Single-Ended (LVPECL)

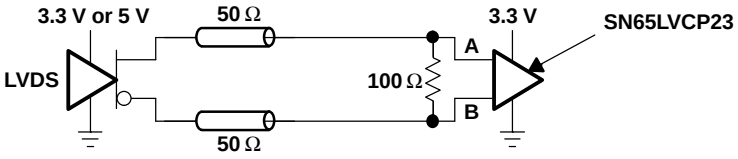


Figure 19. Low-Voltage Differential Signaling (LVDS)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVCP23D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP23DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP23DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP23DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP23PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP23PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP23PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP23PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

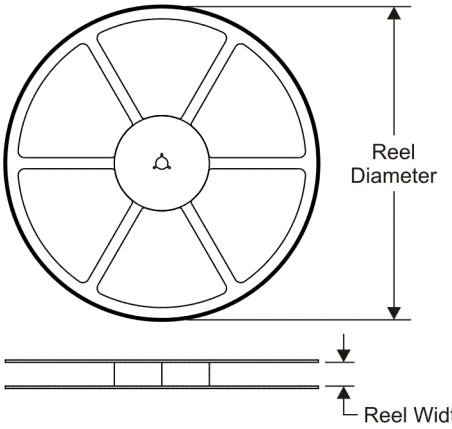
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

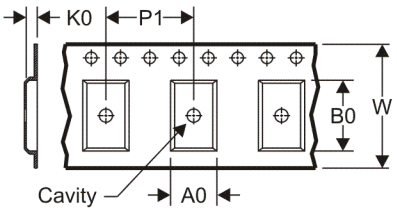
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

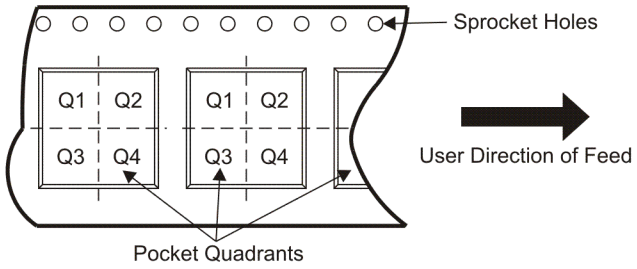


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

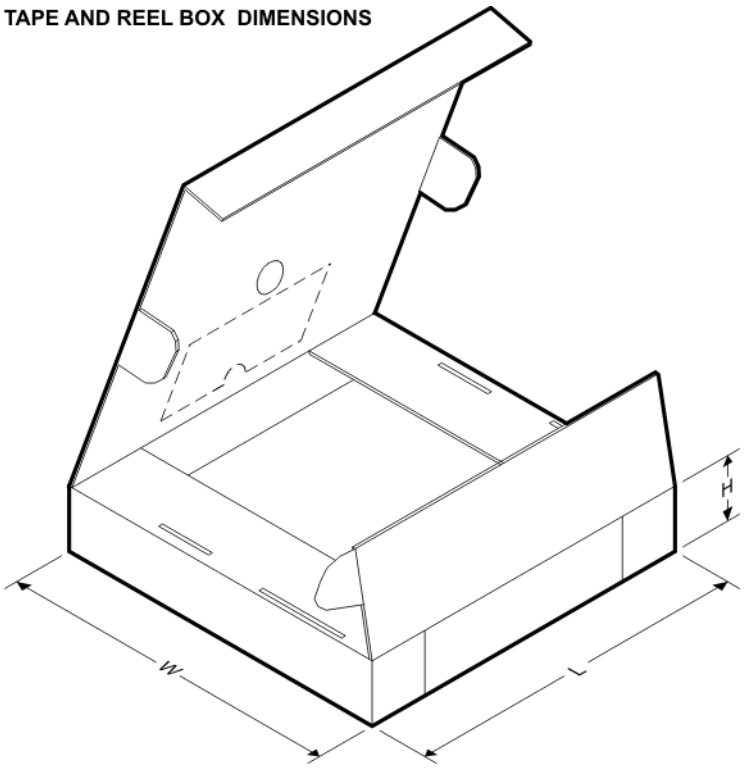
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVCP23DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVCP23PWR	TSSOP	PW	16	2000	330.0	12.4	6.67	5.4	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

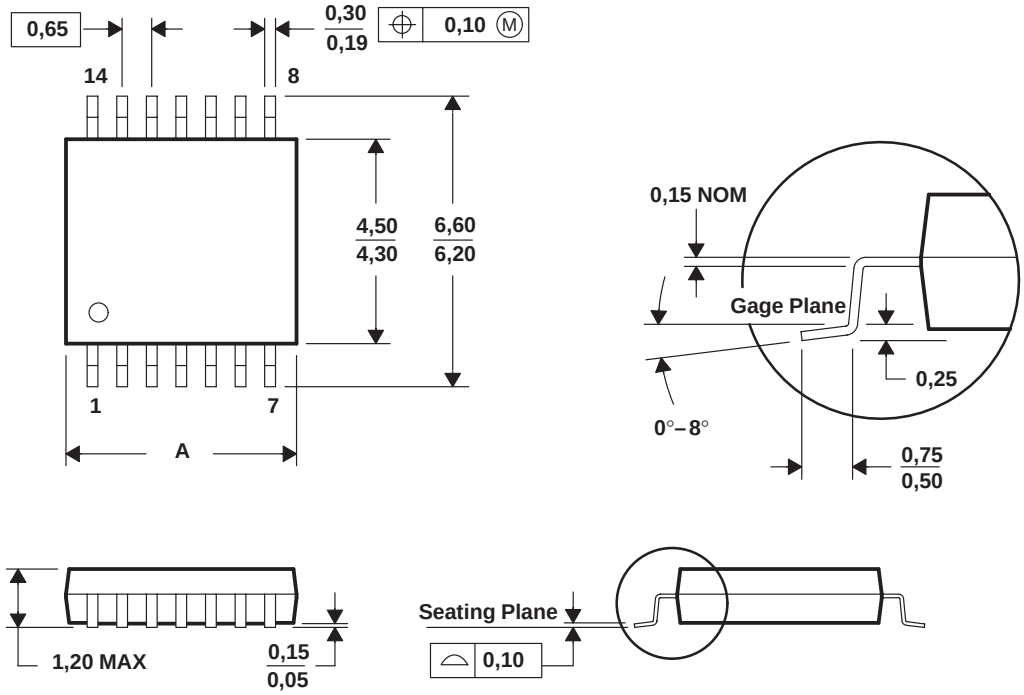


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVCP23DR	SOIC	D	16	2500	346.0	346.0	33.0
SN65LVCP23PWR	TSSOP	PW	16	2000	346.0	346.0	29.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

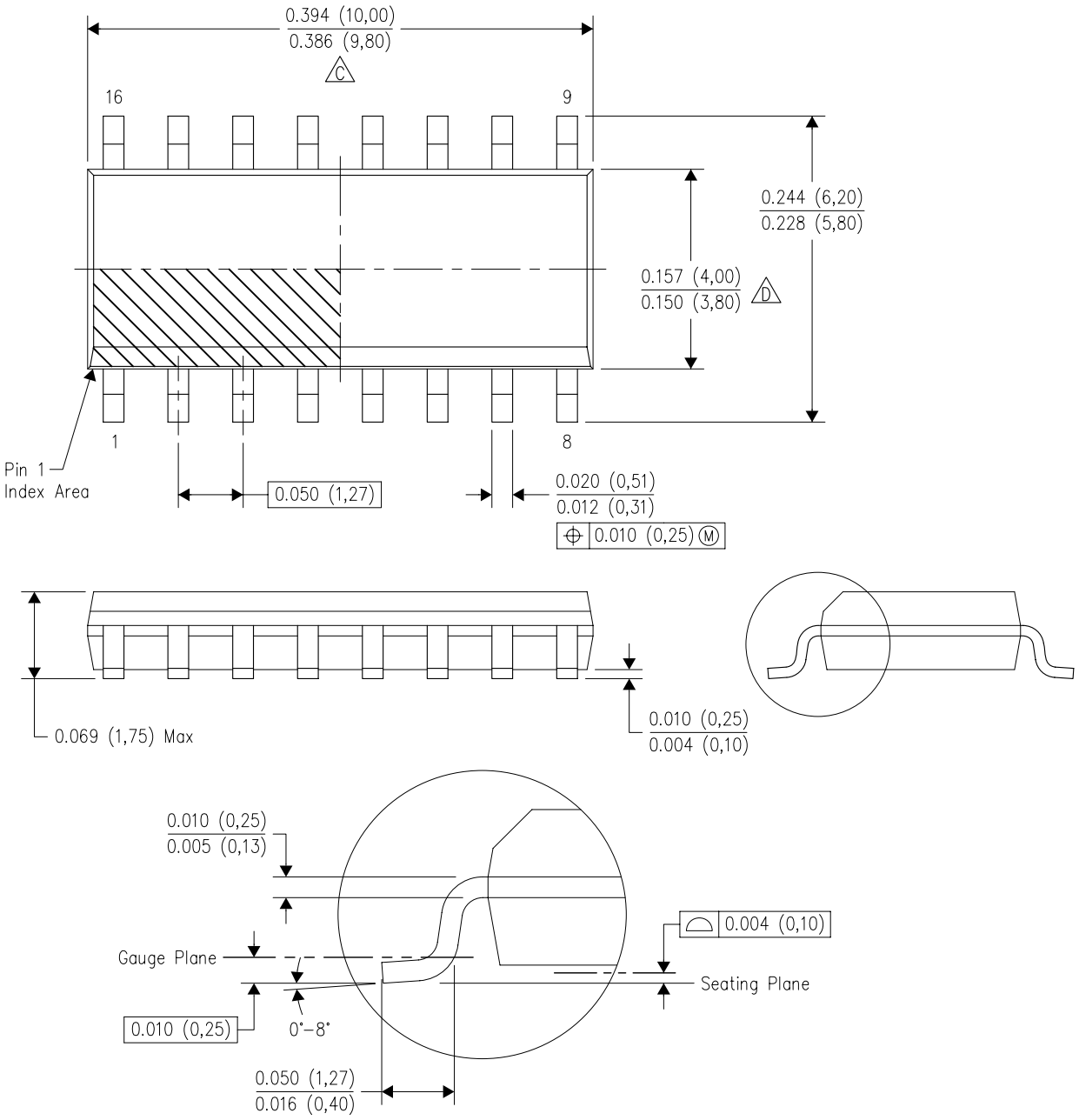


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

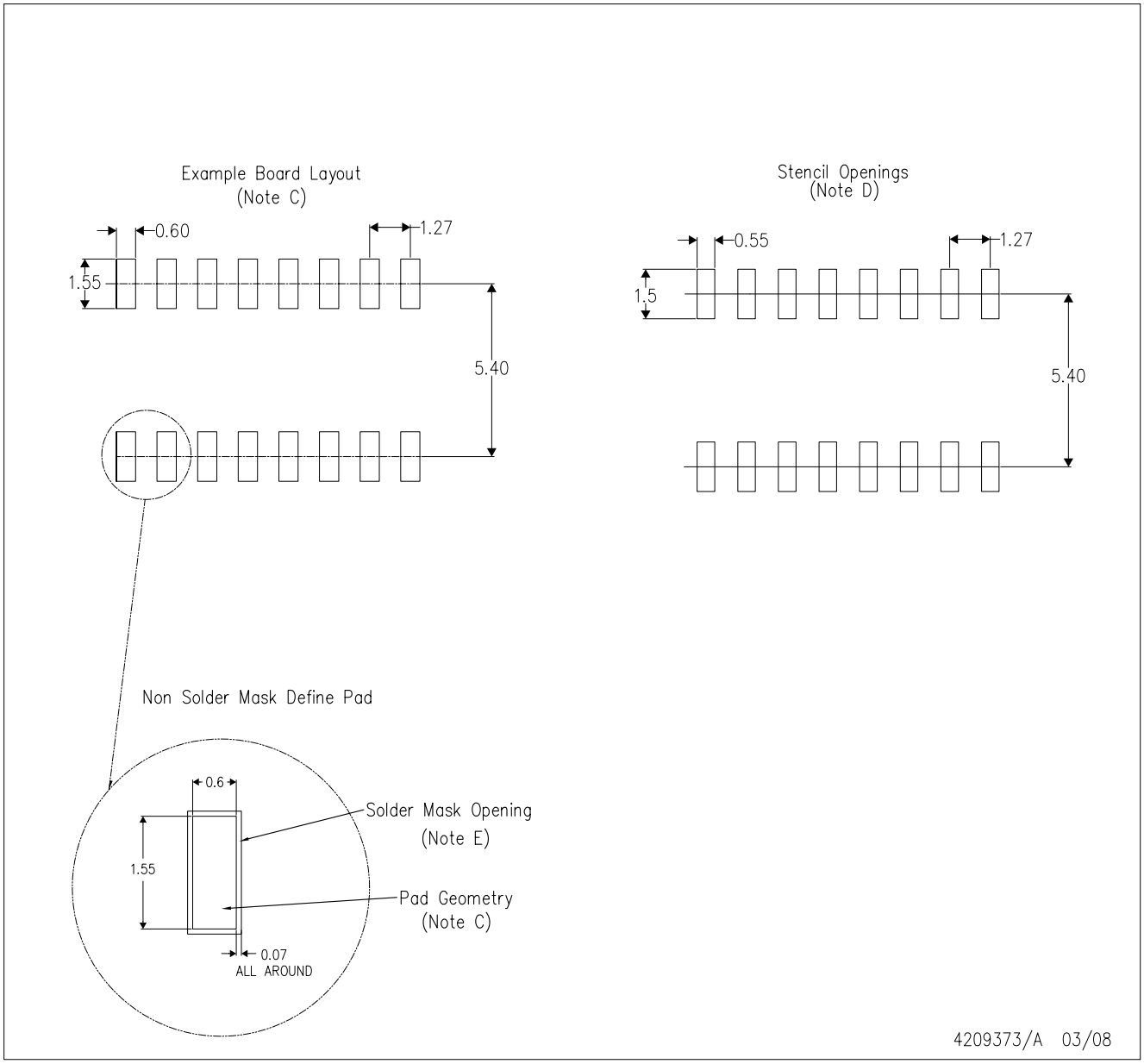
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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